GaAs ICs for 5 GHz Microwave Landing System front-end

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ABSTRACT

The full integration of the 5 GHz front-end of MLS (Microwave Landing System) equipment shows the maturity of the GaAs ASIC design. All the different functions as amplifiers, switches, oscillators, mixers have been integrated as well as digital functions needed for fractional divider frequency synthesis. All the designed ASICs fully comply with specifications and allow the equipment to run in a military environment. The results in terms of spectral purity are very satisfactory.

INTRODUCTION

THOMSON-CNI had to develop an equipment gathering different functionalities (VOR, ILS, MLS...).

In the Microwave Landing System ,ground station transmits horizontal and vertical sweping beams. The localisation is obtained by determining the moment when the aircraft detects the crossing of the beam. Ground stations being located at various distances, the equipment must have a good amplitude linearity over a wide dynamic range to allow a precise determination of the middle of the beam.

MLS can use 200 channels 300 kHz apart, between 5037 and 5097 MHz.

The low volume available in equipment demands a high level of integration.

ARCHITECTURE

It is described in fig. 1 and uses five GaAs chips on a 2 square inch hybrid.

- Input amplifiers and switches.
- mixer and oscillator.
- prescaler by four.
- 41/42 divider plus phase comparator.
- accumulator for fractionnal divider control.

1. Low Noise Input Amplifiers

The circuit selects one out of three antennae or an internal noise generator for built-in-test purpose. The amplifier has a gain control command. Transistor with threshold of -3.5V has been used for achieving a good dynamic range.

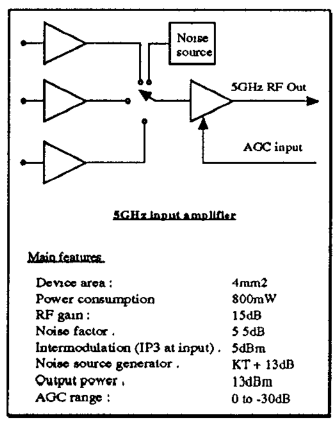

Fig.1 : Input amplifier

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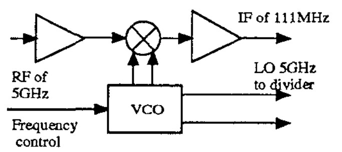
2. Oscillator and mixer

The symetrical oscillator delivers an OL signal for the active mixer, and a symetric output for the prescaler. Inductors and varicaps are integrated on the chip. An external inductor allows the tuning of frequency over ± 10%. Measurements show a very good spectral purity.



VCO - Mixer Ic vith integrated varicap and resonnator

Main features

Device area :	2.2mm2
Power consumption :	900mW
Conversion gain :	0dB
Noise factor :	12dB
Intermodulation (IP3 at input) :	15dBm
VCO frequency :	5GHz
Frequency control :	400MHz
Output power :	2* 0dBm
Spectral purity at 100KHz :	-93dBc/Hz

Fig.2 : VCO-Mixer

3. 41/42 counter and by four divider

The phase locked loop synthetis with fractionnal divider uses a 30 MHz quartz reference. The VCO frequency (F0) is monitored by the digital word (K) at the input of the accumulator.

$$F0 = 4 * (41 + K/400) * 30 \text{ MHz}$$

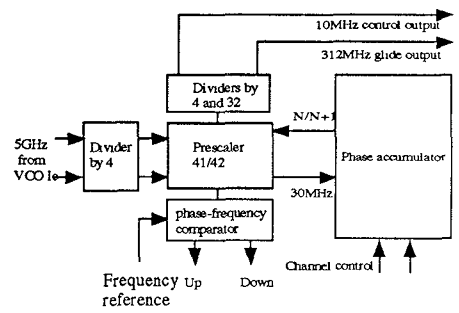
$$= 4920 \text{ MHz} + K*300 \text{ kHz}$$

The by four divider uses .5µ FET in a CML structure.

The 41/42 divider is made of a 5/6 divider followed by a one to eight divider.

Power consumptions are minimized using different types of BDCFL circuits and DCFL as often as possible.

Equivalent spectral purity is better than 135 dBc/Hz at 50 kHz at the phase comparator input stage.



3 ICs based digital frequency synthesizer

Main features

DIVIDER BY 4 (40 Fets)

Device area :	1mm2
Power consumption :	250mW

PRESCALER (250 Fets)

Device area :	3mm2
Power consumption :	120mW

PHASE ACCUMULATOR (700 Fets)

Device area :	4mm2
Power consumption :	120mW
Fmax : :	150MHz

Fig.3 : digital frequency synthetizer

4. Accumulator

The accumulator uses a DCFL structure that leads to a very low power consumption and a maximum operating frequency of 150 MHz.

DESIGN AND REALISATION

Analog circuits have been simulated on a Sun-workstation with a time-based simulator taking into account non-linear effects. Lay-out, checks, and parasitics extraction softwares are from VALID.

Medium complexity digital circuits are checked on digitals simulators. Digital libraries have been created and characterised using modelisation on PSPICE. Final stage of the design is a global analog simulation after extracting the electrical schematics from the lay-out.

Small change of the design was necessary to meet the temperature specifications (-55 + 125°C).

Yield on wafer varies between 50% to 80% according to the chip complexity.

CONCLUSION

Fifteen months after setting up the specifications, the first MLS prototype has been delivered to the customer for flight experiments.

The 5 GHz front-end is a two square inches hybrid with 5 GaAs integrated circuits. This module receives the frequency to be synthesized into a digital form and performs

- the selection of the antenna or the internal noise source for built-in test.
- the synthesis of the local oscillation.
- the mixing towards the 100 MHz IF.

The only external components are the 5 GHz filter and the low-frequency part of the phase lock loop. The features to be specially noticed are:

- the low phase-noise of the 5 GHz VCO with integrated resonator and varicap.
- the low power consumption of the 41/42 prescaler with 1.25GHz input frequency.
- the low phase-noise of the synthesized frequency with GaAs counters and phase-frequency comparator: -95 dBc at 50 kHz of the 5 GHz carrier.
- The large integration level.

Philips Microwave Limeil (France) has realized the chips with a standard technology using On and Off Mesfets with gate length from 0.7 µm to 0.5 µm. It has been possible to reach this level of integration with a good yield, thanks to the good quality of the models inclu-ding non-linearities and our strict design methodology.

For cost, consumption and volume reasons we are now planning to use GaAs ASICs in all our future microwave equipments.

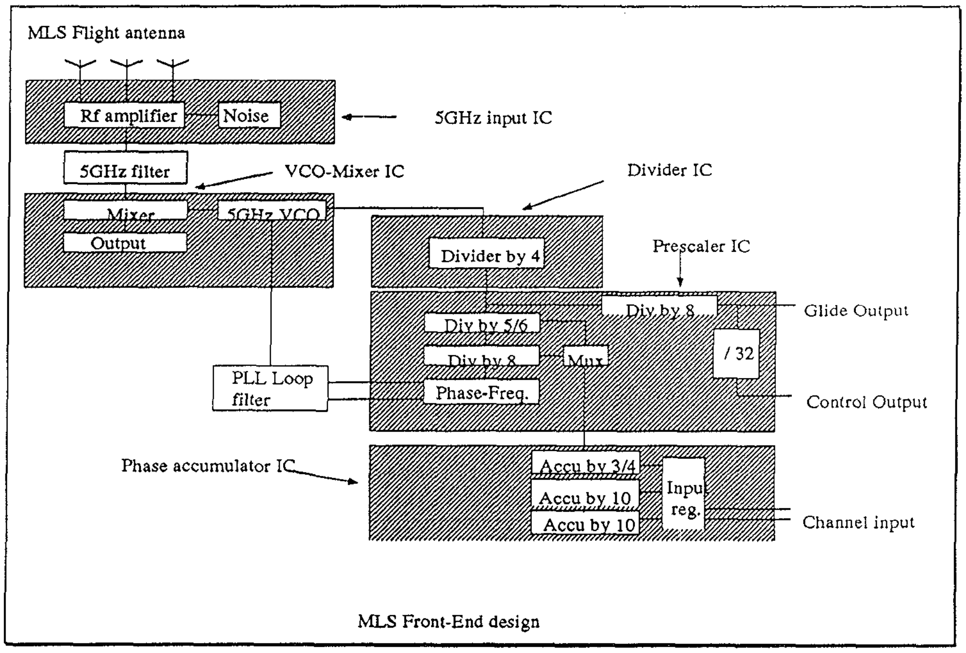


Fig. 4: MLS Front-End architecture